AMENDMENTS TO THE CLAIMS

Claims 1-26. (Canceled)

27. (Currently amended) A ~~processor-based~~ processor system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising:

a fully-depleted SOI NMOS transistor as part of a memory array, said fully-depleted SOI NMOS transistor comprising first source and drain regions provided on a SOI substrate, said first source and drain regions being of n-type conductivity; and a first gate stack fabricated on said SOI substrate, said first gate stack including a doped silicon/germanium layer of p-type conductivity; and

a partially-depleted SOI NMOS transistor as part of a periphery array, said partially-depleted SOI NMOS transistor comprising second source and drain regions provided on said SOI substrate, said second source and drain regions being of n-type conductivity; and a second gate stack fabricated on said SOI substrate, said second gate stack including a conductive layer of n-type conductivity.

Claims 28-31. (Canceled)

32. (Currently amended) The ~~processor-based~~ processor system of claim 27, wherein said conductive layer is a doped polysilicon layer.

33. (Currently amended) The ~~processor-based~~ processor system of claim 27, wherein said conductive layer is a doped silicon/germanium layer.

34. (Currently amended) The ~~processor-based~~ processor system of claim 27, wherein at least one of said first and second gate stacks further comprises a silicide layer over said conductive layer.

35. (Currently amended) The ~~processor-based~~ processor system of claim 27, wherein at least one of said first and second gate stacks further comprises a cap layer over said conductive layer.

Claims 36-86. (Canceled)